AMENDMENTS TO THE SPECIFICATION

Page 4, lines 14 - 16.

Figures 5A – [[5F]] 5E are schematic cross-sectional views illustrating the steps in one embodiment of a process for fabricating a NAND flash memory cell array in accordance with the invention.

Page 6, line 26 to Page 7, line 2.

The memory cell array of Figures 2 - 4 can be fabricated by the process illustrated in Figures 5A – [[5F]] 5E. In this process, an oxide layer 53 is thermally grown to a thickness of about 70Å to 200Å on a monocrystalline silicon substrate which, in the embodiment illustrated, is in the form of a P-type substrate 41 in which a P-type well 52 is formed. Alternatively, if desired, an N-type well can be formed in the P-type substrate, in which case the P-type well will be formed in the N-type well.

Page 8, lines 20 - 24.

Thereafter, a glass material [[60]] such as phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG) is deposited across the entire wafer, then etched to form openings for bit line contacts 46[[, as shown in Figure 5F]]. Finally, a metal layer is deposited over the glass and patterned to form bit lines 57 and bit line contacts 46.